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Analysis of Digital Signal Processing Algorithms Based on Vedic Mathematics

A.Lisha[*1], T. Monoth[2]

Department of Computer Science, Mary Matha Arts & Science College, Kannur University, Mananthavady, Kerala
**Corresponding Author:lisha84@gmail.com, Tel.:+91 9847571254*

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***Abstract*—** India has a rich intellectual tradition that evolved since last 5000 years. To our luck much knowledge acquired over this period were kept as ancient scriptures. Vedic Mathematics is the name given to the ancient system of Indian Mathematics which was rediscovered from the vedas by Sri Bharathi Krishna Tirthaji. The whole vedic mathematics is based on sixteen sutras providing unique and simple techniques to various mathematical computations. Processing time, power and hardware are the main challenging aspects in any computer algorithms. Hence high speed mathematical tools are of great demand. Ancient Indian scripts are believed to contain many mathematical shortcuts which can be used to fine-tune computer algorithms. Many researchers found the Vedic multipliers, adders and other vedic tools help in saving resources. In this paper we present various applications of vedic mathematics in Digital Signal Processing and also analyzed computational complexity of various algorithms in digital signal processing using vedic mathematics proposed by different researchers.

***Keywords*—** Vedic Mathematics, Vedic Sutras, Urdhva Tiryakbhyam Sutra, Digital Signal Processing

I. INTRODUCTION

Ever since computer algorithms were evolved, techies were after the ways to optimize the speed and performance of the algorithms to the maximum possible extend. Vedas – The treasures of knowledge attracted many enthusiastic scholars who were focused to this area. Rigveda , the oldest of four vedas comes to picture because of the mathematical element in it. A Hindu scholar named Shri Bharati Krishna Tirthaji, who was also a mathematician, rediscovered sixteen sutras which are easy short cuts for long mathematical calculations. This paper is a review of various researches carried out to improvise computer algorithms using the vedic mathematics sutras with a special focus to Digital Signal Processing (DSP). Speed improvement in DSP is considered to be challenging. Vedic mathematics methods can be directly applied for DSP computations.

This paper is organized is as, Section II describes the vedic mathematics and explanation of Urdhava Tiryakbhyam sutra. Section III describes application of vedic mathematics in DSP algorithms. Analysis of computational complexity of different algorithms using vedic mathematics presented in section IV and conclusion offered in section V.

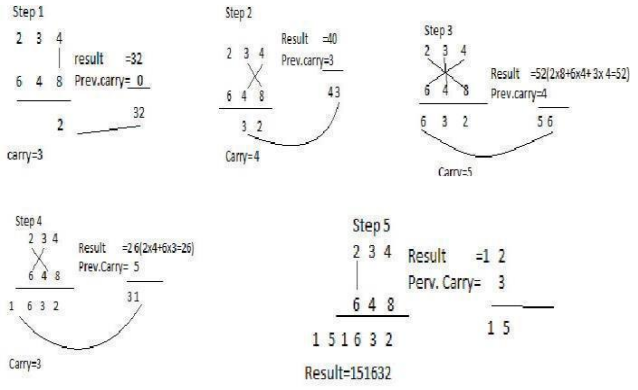
II. VEDIC MATHEMATICS

Multiplication and divisions of large numbers would involve long mathematical calculations. Such long calculations can be curtailed using vedic mathematical shortcuts. There are 16 sutras and 15 subsutras which are mathematical shortcuts according to Tirthaji [1]. Out of them urdhva tiryakbhyam sutra is more efficient to reduce number of operations for multiplication of large figures.

A. Urdhva Tiryakbhyam Sutra

Urdhva Tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication which means „vertically and crosswise". To illustrate the multiplication of two decimal numbers with example line diagram for the multiplication is given below. e.g. 234x648

Initially the LSB digits on the both numbers of the line are multiplies and added with the carry from the previous step. This generates one of the bits of the result and carry. This carry is added in the next step and the process goes on likewise. When there are more lines in one step, all the results are added to previous carry.



Since there is a parallel generation of the partial product and their sums, the processor becomes independent of the clock frequency. The advantage here is that parallelism reduces the need of the processor to operate at increasingly high clock frequency and this optimizes the processing power [2]

III. VEDIC SUTRAS IN DIGITAL SIGNAL PROCESSING

A research done by P. Saha et al. [3] is about the implementation of vedic shortcuts in DSP. This study deals with the reciprocal approximation and divisions in DSP. The reciprocal approximation method is conventionally based on Newton Ralphson iteration method. Here vedic formulae are used by transforming the digits to smaller digits and entire division are carried out through the transformed digits. When the vedic sutras are used it was observed that number of iterations reduced and thus resulted the reduction of propagation delay and dynamic switching power consumptions. A research carried out by R. Jamgade et al. [4] is about Psudo Noice sequences which serve as an extra security measure for wireless communication signals. The conventional PN generator used is Galios multiplier and here it is proposed to be replaced by vedic multiplier. The results of their study show vedic multiplier to be efficient in terms of speed and space consumed.

A. Savadi et al. [5] in their research a 64 bit Infinite Impulse Response (IIR) filter has been implemented using Urdhava Tiryakbhyam Sutra of vedic mathematics. IIR is a digital filter. They found that the proposed IIR filter in which vedic sutras are used, takes less processing time compared to conventional method. Implementation of 64 Bit High Speed Multiplier for DSP Application – Based on Vedic Mathematics [6] is a research paper published by Jinesh S et al. As a result of their study they propose a new architecture for high end processor for better performance. They have identified that the multiplication operation in functions like Fast Fourier Transform (FFT), Discrete Cosine transform (DCT) are the resource consuming areas which could be optimized with vedic sutras. The proposed system is a new 64 bit vedic multiplication system combining four 32 bit vedic multipliers. The results of their study state that the vedic multiplier gives better speed than other multipliers like booth and Wallace tree multipliers.

S.N. Gadakh et al. [7] propose a 16 X 16 bit vedic multiplier architecture using urdhva tiryagbhyam sutra of vedic mathematics. The advantage of the new multiplier is that the partial product generation and addition happen simultaneously. So it suits best for parallel processing. The proposed vedic multiplier is implemented in adder circuitry. Three different types of adders are used in the architectures, namely ripple carry adder, carry select adder and carry save adder. When they compared the simulated performance of proposed architecture it shown 33.26% reduction in combinational path delay.

The Floating Point Multipliers (FPM) are critical delay path components in DSP processers. Here Anjana S et al. [8] discuss the design of a high speed energy efficient FPM. In the proposed system they use a vedic multiplier using Carry Look Ahead Algorithm (CLA) and Ripple Carry Algorithm (RCA). The vedic multipliers are found to be having more speed than other multipliers. Mohan Shoba et al.[9]proposes new hierarchy multiplier architecture based on vedic mathematics. They found from the simulation results that the proposed vedic multiplier is efficient in terms of area, time and power consumption.

L P Thakare et al. [10] proposed a complex floating point multiplier based on vedic mathematics. Complex floating point multiplier is used when complex operations occur with respect to the real and imaginary numbers together. The proposed system can be used in a Fast Fourier transform. The designed complex floating point multiplier can be work for any floating point numbers within range of single precision format. The proposed system provides cost effective solution for DSP applications. The proposed system is also area efficient. N R Punwantwar et al.[11] proposed a method for calculating the linear convolution and De-convolution with the help of vedic mathematics. The main module for performing convolution and de-convolution is multiplier and divider. Urdhava Tiryakbhyam sutra is used for multiplication and paravartya sutra is used for division. The execution time of proposed method for convolution is reduced by approximately 28% than the convolution using conventional multiplier. The execution time for de-convolution is provides 30% improvement than non-restoring algorithm. Deepthi P et al [12] in their paper they discussed about the design of an 8 bit fixed point, asynchronous vedic DSP processor core. In their work they used Urdhava tiryabhyam, Nikilam, Ekadhikena Purvena, Ekanyunena Purvena, Anurupyena Antyayor Dasakepi sutras in vedic mathematics. The proposed vedic DSP contains a data pre-processing block, ALU with vedic multiplier and divider, barrel shifter and register bank .It reduce 40% of the power consumption.

IV. ANALYSIS OF COMPUTATIONAL COMPLEXITY USING VEDIC MATHEMATICS

To evaluate the performance of vedic mathematics algorithms researchers recommended various parameters such as time, delay, power and number of slices. Here we analysed computational complexity of algorithms using vedic mathematics proposed by different researchers are given in table 1.

Table1. Performance Analysis of vedic Algorithms

S. No	Author/ title of the Paper	Vedic sutra applied	Computational Complexity
1	P Saha, D Kumar et al [3]	Applied in transition level implementation technique of reciprocal unit	Reduction of Circuit level complexity And reduction in propagation delay
2	Roshni Jamgad e et al[4]	Applied in Psedo Noise sequence	Reduced delay, Space and speed is high
3	Anuradha Savadi et al [5]	Applied in convolution of designing IIR filters.	Less average processing time
4	Jinesh S et al [6]	Applied in 64 bit multiplier	Efficient in Terms of computational delay and area
5	Sheetal N Gadakh et al [7]	16x16 Bit Multiplier Design	Optimization of memory requirements, Efficient in speed
6	Anjana S et al [8]	Applied in floating point multiplier	Efficient in terms of area, power delay
7	Mohan Shoba et al. [9]	Applied in hierarchy multiplier.	Better speed and efficient in area
8	L P Thakare et al. [10]	Applied in FFT.	Efficient in Terms of accuracy and speed.
9	N R Punwantw ar et al. [11]	Applied in convolution and de-convolution	Faster working and low power consumption
10	Deepthu P et al. [12]	Applied in DSP Core.	Efficient in Time and power consumption

By the analysis from the table we see that by using Urdhva Tiryakbhyam Sutra for multiplication the algorithms are efficient in time, area and power.

V. CONCLUSION

In this paper, we analyzed various researches carried out to use vedic sutras in computer algorithms with a special focus to the digital signal processing. All the researchers recommend the use of vedic shortcuts in algorithms to save hardware resources and processing time. In future these sutras can be applied for other signal processing algorithms, and researches towards the usage of remaining vedic sutras can be of great advantage.

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Authors Profile

Mrs. A Lisha, Assistant Professor, Department of Computer Science, Mary Matha Arts & Science College, Mananthavady, Kerala. Her interests are Digital signal processing, Digital image processing, Vedic Mathematics, etc.

Dr.T. Monoth, Head, Department of Computer Science, Mary Matha Arts & Science College, Mananthavady, Kerala and Research guide, Department of Information Technology, Kannur University, Kannur, Kerala. His interests are Visual Cryptography, Secret Sharing, Image Security, etc.